Voodoo 4 & 5
BIOS REVISION HISTORY

Versions 0.01 – 1.06

Document Name : Voodoo 4 & 5 (VSA-100 Series) BIOS Revision Guide
Original Date : Produced – 25th August 2001
Last Update : Updated – 25th August 2001

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Overview : Since the first release of the Voodoo4 and Voodoo5 BIOS's on the V3Info website, there has been huge controversy over their authenticity, this document doesn't apply to those over 1.06 but it does cover a significant amount. Many of the BIOS's mentioned in this document are Pre-Production BIOS's, but it does show that 3dfx was indeed refining the BIOS's since the 1.00 version. This document is far from complete and does not prove the authenticity of the 1.15, 1.16 and 1.18 BIOS's, but this may be added at a later date.

Availability : This document will be available from any site within the V3Info.co.uk / Voodoosource.net partnership. To find out if you can host this document on your site, you should contact Wipeout at Wipeout@Voodoosource.net.

Thankx : The following people should be commended due to their dedication with V3Info.co.uk and the Voodoo BIOS adventure.

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And finally, all the staff members involved in V3Info.co.uk and Voodoosource.net.

Comments? : Please send any and all comments to AMDFreak@BTInternet.com

Leechers? : If you downloaded this document from anywhere other than www.v3info.co.uk / www.v3info.de / www.voodoosource.net please report it to AMDFreak@BTInternet.com.

***** Napalm Release Note *****

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5/15/00 - Ver. 1.06
Set VidProcCfg[29:28] = 11 to disable memory optimization.

* OEMPOST.ASM *
In InitRegisters, set VidProcCfg[29:28] = 11b.

* OEM.ASM *
In OemSetRegs, did a Read-Modify-Write of VidProcCfg. Preserved bits 29-28.

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5/08/00 - Ver. 1.05
Corrected VPD Checksum to allow for (ICT) Production BIOS programming

* MAIN.ASM *
Changed VPD Checksum from 0x85 to 0x79

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5/03/00 - Ver. 1.04
Disabled PCI memory retries, PCIInit0[12]=1, to fix problem with dropped pixels in VGA mode.

Updated MCLK PLL and DramInit settings.
Current Settings are as follows:
MCLK = 166MHz (E721h)
DramInit0 = 001EA9B9h
DramInit1 = 00240031h

Disabledd sync on slave chips only on 2-way and 4-way boards.

* OEM.INC *
Changed PCIInit0 = 01841320h, 166MHz MCLK PLL = E721h, DramInit0 = 001EA9B9h, and DramInit1 = 00240031h.

* OEMPOST.ASM *
In OEMInitBIOS, added conditional compile code to disable the sync on the slaves chips only on 2-way and 4-way BIOSs.

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4/13/00 - Ver. 1.03

* OEM.INC *
To improve performance, changed the DramInit0 value to 00116A9A9h

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4/13/00 - Ver. 1.02
Created a BIOS to run the part at 166MHz. Changed the default MCLK to 166MHz and the DramInit1 setting to 00240031h.

* OEM.INC *
changed the MCLK setting to 166MHz, 720Dh, and the DRAMInit1 setting to 00240031h

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4/5/00 - Ver. 1.01
Fixed problem with DDC read errors on LG Flatron 759-FT CRT monitor.

Updated the CLK PLL settings for NTSC and PAL 800x600.

Modified TV code to always disable the CRT when TV is active. CRT is disabled by setting MiscInit1[8]=1, Power down CRT DAC.

Added code to disable the TV interface, vidInFormat[15] = 0, when TV or DFP is not active. Fixes problem with TV showing garbage when TV is disabled and CRT is enabled.

* CLKPLL.INC *
Changed the PLL setting for 36MHz, PAL 800x600 TV clock, and 38.769MHz, NTSC 800x600 TV clock.

* VESA.ASM *
Added additional clock delays to the DDC routines. This fixes the problem with reading DDC information from LG Flatron 759-FT CRT monitor.

* OEM.ASM *
In OEMSetRegs, disabled the TV interface when TV or DFP is not active.

In OEMSetRegs, diabled the CRT when TV is active.

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3/24/00 - Ver. 1.00
Changed the default DramInit timings for 143MHz MCLK.
DramInit0 = 00016A9B9h
DramInit1 = 000200031h
PLLCtl1 (MCLK) = 3A05h = 143MHz

Fixed problem with some default BIOS modes PLL value causing the mode to "swim". Updated the PLL values for the following VBE modes: Extended Text Modes 109h-10Ch, 320x200, 320x240, and 512x384. Also adjusted the PLL setting for the TV modes.

Changed the sign-on message to report the total amount of memory on board. This includes the memory on the slave chips.

Added a 128 Meg memory entry into the memory size string.

* CLKPLL.INC *
-= NEW FILE =-
Include file which holds the equates of all the VGA and VBE
mode clock PLL setting.

* OEMDATA.ASM *
Made all the CLK PLL setting into equates and put the equates into
CLKPLL.INC.

Updated the memory size strings to include a 128 Meg entry.

Modified the SDRAM and SGRAM memory message strings to say "Total SDRAM " and 'Total SGRAM "

* OEM.INC *
Changed memory clock to 143MHz PLLCTRL1=3A05h and DramInit0 = 00016A9B9h
and DramInit1 = 000200031h.

* OEMPOST.ASM *
In OEMSignOn, adjusted the reported memory size depending if we're a
4-way or 2-way SLI board.

* MAKEFILE *
Added CLKPLL.INC as part of the dependencies for OEMDATA.ASM.

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2/24/00 - Ver. 0.34
Changed the PCIInit0 setting from 0184FB20 to 01840320h.

Forced DramInit0[30] = 1 to always do SDRAM even thou we're running on SGRAM.

* OEM.INC *
Changed DEFAULT_PCIINIT0 to 01840320h.

* OEMDATA.ASM *
Made the variable fBoardConfig public.

* OEM.ASM *
Modified the routine CheckIfSGRAM to use the variable fBoardConfig instead of testing DramInit0[30].

* OEMPOST.ASM *
In InitRegisters, always set DramInit0[30]=1 to force SDRAM.

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2/17/00 - Ver. 0.33
Changed the PCI Empty low water mark, PCIInit0[6:2], from 0x01 to 0x08.

Changed the BIOS dot clock algorithm for finding PLL settings.
This change only effects GTF modes and scaled panel support.
This fix addresses PRS#12553 and #12555

* OEM.INC *
Changed the DEFAULT_PCIINIT0 from 00584FB04h to 00584FB20h.

* OEM.ASM *
In SetAbsoluteDotClock, removed the software work-around which patch PLL settings to get hi-res modes to work.
This work-around was for PRS #12553 and #12555.

In CalcClockWord, updated the algorithm for finding PLL settings for a specified dot clock.

Created the routine CheckVCO to validate PLL setting before they are used.

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2/8/00 - Ver. 0.32
Changed BIOS chip name string to "VSA 100".

Fixed bug in CheckForPanel routine. Would always return panel attached, even though no panel is attached.

Fixed bug with DFP/TV combo BIOS not booting to TV only properly.
Fixes PRS#12528.

Removed unnecessary XLCD code and DFP I2C routines.

* OEM.INC *
Change the STR_OEMCHIPNAME string to "VSA 100".

* OEM.ASM *
Removed the routine I2CWriteRegister_Panel. Not needed since Napalm uses DDC calls.

* OEMPOST.ASM *
Removed the extrn for I2CWriteRegister and added an extrn for DDCEnableDFP.

In CheckForPanel, called the routine DDCEnableDFP to enable access to the DFP. Removed old XLCD code.

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2/2/00 - Ver. 0.31
Fixed bug with Flight Simulator 5.0 showing garbage when moving around the mouse cursor during a game.
Fixes PRS#12642

* OEM.ASM *
In OemSetWBank, did a PUSH and POP EBX at the start and end of the routine.

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2/2/00 - Ver. 0.30
Changed the name of the routine I2CReadByte to DFPReadByte. This routine now uses DDC calls to read DFP EDID data. This change fixes the problem with detecting scaled and non-scaled DFPs and also scaled DFPs now fully supported. Also fixes problem with scaled DFP not coming up in VGA modes.

* OEM.ASM *
Renamed all the calls to I2CReadByte to DFPReadByte.

DFPReadByte now uses DDC calls to read DFP EDID data.

* OEMPOST.ASM *
Renamed all the calls to I2CReadByte to DFPReadByte.

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1/28/00 - Ver. 0.29
Modified DFP DDC code to use DDC code instead of the I2C code.

Fixed bug with DDC code not sending a NACK after reading last byte.

Addressed the following PRS:

#12558 - 320x200x8bpp locks the system when attempting to set 60hz or 65hz in VBETEST.

#12553 - 1024x768x8@90Hz shows incorrect refresh rate.

#12555 - 1280x1024x8@65Hz and 70Hz show incorrect refresh rate.

* OEM.ASM *
In PatchVertDisplayTime, fixed bug with BIOS being stuck in an infinite loop if vertical total bit 9 = 0.
Fixes PRS#12558.

In OEMDDCDisable, changed the AND mask to 09FFBFFFFh to also reset the GPIO port back to 00.

Created the routine DDCEnableDFP to setup the DDC calls to the panel. This includes setting up the GPIO port to read DDC data from the DFP.

In SetAbsoluteDotClock, created a software work around to fix the porblem with certain PLL settings causing th PLL to not generate the desired output frequency.
Address PRS #12553 and #12555.

* VESA.ASM *
Removed the routine ReadFP_EDID and calls to this routine.

In DDCStartupSequence, added code to check for an attached panel. If a panel is attached, call DDCEnableDFP to setup the DDC call to read DDC data from the DFP.

In DDCRead, placed a PUSH CX and POP CX around call to DDCWaitClockHigh. Fixed bug with a NACK never being sent to the monitor after reading the last byte of DDC data. This enables the BIOS to read DDC data from a Compaq FP720 DFP.

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1/21/00 - Ver. 0.28
Fixed bug in DOS extended mode Write TTY and scrolling function.

For DFP only, set tmuGBEInit[18]=1 to select a delay of 4. Also set VidInFormat[22] to disable tv_data_scramble. This fixes the problem with wrong colors on the panel.

Fixed bugs in bank switching code.

Fixed bug with boot on TV only.

Added work-around to memory VBE memory size routines. BIOS VBE memory sise functions will return 16 Meg on board when running on 32 and 64 Meg boards.

Changed board designs #872, #882, #883, and #884 from SGRAM to SDRAM.

* OEM.ASM *
In FixupPanel, set tmuGBEInit[18]=1 to select delay of 04h. Also set VidInFormat[22] to disable tv_data_scramble to fix the problem with wrong colors on the panel.

In OemGetWBank and OemGetRBank, fixed bug with not properly getting bits 11 and 10 of the apperture.

Removed the routine CheckIfProduction. Not needed in Napalm.

* OEM.INC *
Changed the build options for board designs #872, #882, #883, and #884 from SGRAM to SDRAM.

* OEMDATA.ASM *
In VBEPMI05, code needed to be modified to handle Napalm's defination of appeture in VGAInit1.

* OEMPOST.ASM *
In OemNoMonitor, removed the call to checkIfProduction from the TV portion of the code.

* SCROLL.ASM *
Modified all the routines which called the bank switching routine to pass DX and not just DL.

* VESA.ASM *
In VBE_ReturnControllerInfo and VBEGetmemSize routines, changed the memory size routine to return 16 Meg on board when running on 32 and 64 Meg boards.

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1/15/00 - Ver. 0.27
Create build options for Napalm board Assy# 879, 880, 881, 882,
      883, and 884.

Changed device ID to 09h

Fixed bug with TRS BIOS hanging

Fixed memory sizing bug.

* OEM.INC *
Changed device ID to 09h

Changed the following parameters:
      DramInit0 = 00169D25h
      DramInit1 = 00046C031h
      MCLK = 02805h

* OEM.ASM *
In Find3DFXCard, added check to see if running TRS BIOS before
doing SSID check. Will skip SSID check if TRS BIOS.

* OEMPOST.ASM *
In InitRegisters, Changed the DramInit0 mask to not clear DramInit0[26].
Fixed memory sizing error.

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1/11/00 - Ver. 0.26
Create build options for Napalm board Assy# 874 and 872.
Updated the copyright year to 2000.
      "Copyright (C) 1990-2000 Elpin Systems, Inc."

* OEM.INC *
Create build options for Napalm board assy #874, -DBUILD_V5P874,
and #872, -DBOARD_V4P872.

* DATA.ASM *
Updated the copyright year to 2000.

* MAIN.ASM *
Updated the copyright year to 2000.

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12/16/99 - Ver. 0.25
Overscanned the NTSC 640x350 TV parameters to be full screen on the TV.
Ratio used were HOC = 13.78 and VOC = 9.88.

* OEMDATA.ASM *
Changed the NTSC 640x350 TVDATA table entries to support 640x350
overscanned parameters.

* OEM.ASM *
In FixupTVOut, added code to program the Brooktree TV encoder to
do overscanned 640x350 NTSC timings.

* OEM.INC *
Changed the PCI device to 07h for Napalm.

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12/7/99 - Ver. 0.24
Changed the panel CRTC timings to fix bug with setmode hanging while
in a full screen DOS session in Win98.

* OEMDATA.ASM *
In the tblExtRegisters table, changed the CR11 panel setting for the
following modes to not set CR11[4]. Fixes GPF error when setting
these panel modes.
- 1024x768 panel timings -
Updated timings for all 512x384 modes and 640x400x16bpp.
- 1280x1024 panel timings -
Update timings for modes 07*, 00*, 01*, 02*, 03*, 00/01+, 02/03+,
and 07+.

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11/30/99 - Ver. 0.23
Expand the NTSC 640x400 and 320x200 modes to be full screen on the TV.

Modified build process to support only have needed one compile flag
to build a BIOS.

Updates the OemConfig structure to return the chip name, oem board
name, and version number.

* OEM.ASM *
In FixupTVOut, patched the Brooktree TV timings when doing 640x400 and
      320x200.

* OEM.INC *
Changed the following variables from "EQU" to "=". This make it possible
to change the value of the variable during the compile.
VARIATION_001, VARIATION_002, VARIATION_003, VARIATION_005, ROM_64K,
OPTIMIZED_ROM, FB_High_Priority, TVOUT_BIOS, PAL_BIOS, DVI_BIOS,
MCLK_183MHZ, MCLK_166MHZ

Created the following variables:
BoardI2CLineShorted
BoardCRTSupport
SDRAM_BIOS
BoardMemType
BoardBusType
BoardTVOutSupport
BoardDFPSupport

Moved the STR_OEMPRODUCT into each board compile option. Each build
option has a unique OEM Product string. The BIOS will now print
is the BIOS supports TV or DFP.

Changed the PCI device to 07h for Napalm.

* OEMDATA.ASM *
Modified the NTSC TVDATA structure to use the new 640x400 and 320x200
full screen TV timings.

Update the OEMConfig structure to include the VBE product name,
OEM Chip name, and OEM BIOS version.

Created the null terminated strings for Chip name and BIOS Version.

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10/28/99 - Ver. 0.22
Renamed all the "XLCD" references to "DVI". To build an DVI,
set VGABIOS_OPT=-DBUILD_DVI_BIOS

Added support for new BoardConfig DWORD into new OEMConfig structure.
BoardConfig return information about the boards memory type, bus
type, TV out support, DVI support, CRT support, and if the
I2C lines are shorted.

* OEM.ASM *
Renamed all the "XLCD" references to "DVI".

* OEM.INC *
Added the equates BoardI2CLineShorted, BoardCRTSupport, BoardMemType,
BoardTVOutSupport, and BoardDFPSupport.

Renamed all the "XLCD" references to "DVI".

* OEMDATA.ASM *
Renamed all the "XLCD" references to "DVI".

Created the word variable OEMConfigVer which is right before the
tblOEMConfig label. OEMConfigVer stores the current version of the
OEMConfig table.

Created the variable "Reserved" to word align the variable fBoardConfig
variable.

Created the variable fBoardConfig to store the board configuration.

* OEMPOST.ASM *
Renamed all the "XLCD" references to "DVI".

* VESA.ASM *
Renamed all the "XLCD" references to "DVI".

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10/11/99 - Ver. 0.21
Merged in all the Napalm 0.20 changes onto the StarTeam Napalm BIOS.

Added support for doing 320x240, 400x300, and 512x384 modes centered
on a scaling DFP.

* OEMDATA.ASM *
Created CRTC panel timings for 320x240, 400x300, and 512x384 modes
on a scaled DFP.

* OEM.ASM *
Created externs for the 320x240, 400x300, and 512x384 DFP CRTC timings
in OEMDATA.ASM.

In the FixupPanel routine, for scaled panels only:
1) Disabled scanline doubling. VIDPROCCFG[4] = 0.
2) For the 320x240, 400x300, and 512x384 modes, loaded the 320x240,
   400x300, and 512x384 CRTC timings instead of the 640x480, 400x300,
      and 1024x768 timings.
3) Fixed problem with modes being too far to the right by skewing
   the image to the left by writing MiscInit0 [10:08].

In ProgramCRTCPanelTimings, expanded the CRTC registers which are
   programmed to include CR12, CR09, CR10, and CR11.

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9/9/99 - Ver. 0.19
Fixed problem with halved extended modes (320x200, 320x240, 400x300, and 512x384) not being displayed on the DFP.
NOTE! Currently, the halved modes only use half of the screen horizontally but full screen vertically. The issue with halved extended mode using half of screen horizontally will still need to be addressed.

* BIOSPARM.INC *
Created labels for the 640x480, 800x600, and 1024x768 default timings.
Fixed up the horizontal blank times for all the 800x600 and 1024x768 timings.

* OEM.ASM *
Created externs for the 640x480, 800x600, and 1024x768 VGA tables.

In FixupPanel,
1) Added support for doing 320x200, 320x240, 512x384, and 400x300 modes.
2) Modified the code which patched CR02 to decreament the CR02 value
   by 1 instead of copying the CR01 value. This helped fixing the
   problem with halved modes not coming up.

In ParseAndProgramDetailedTimings,
1) CR01, Horizontal Display End, is NOT updated when in doing a halved
   mode.
2) CR05, Horisontal sync End, is foced to 1Fh for halved modes.

Created the routine ProgramCRTCPanelTimings read and program the CRTC timings in BIOSPARM.INC.

Created the routine IsHalvedExtMode to return if we're a halved extende mode mode.

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9/4/99 - Ver. 0.18
Fixed bug with panel not being enabling scale panels in DOS after setting CR1F=09h.

For a 32K ROM only, the BIOS needed to update the ROM checksum after discarding the POST. Fixes failure with Elpin test T0920.EXE.

* OEM.ASM *
In the FixUpPanel routine, moved the code which set REG_VIDINFORMAT to 8000h to the top of the routine. This ensures that REG_VIDINFORMAT is always set when programming the panel.

* OEMPOST.ASM *
In Patch32KROM, added code to recalculate the BIOS checksum.

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8/30/99 - Ver. 0.17
Modified the Panel EDID routine to use the procedures IsCRTAttached
and IsPanelAttached instead of hard coding the routine to read from
specific registers.

* VESA.ASM *
Modified the panel code in DDCReadEDID to use the routine IsCRTAttached
and IsPanelAttached to see if the device is attached before determining
to read EDID from the panel or CRT.

* OEM.ASM *
Created the routine IsCRTAttached to return if the CRT is active.

Added code into the FixupPanel return to support programming the
CRTC and PLL registers for scaled panels.

Created the routine GetDetailedTimingXYRes to parse a panel EDID
detailed timing block and return the XY resolution for that
detailed timing block.

Created the routine ParseAndProgramDetailedTiming to parse a detailed
timing block, calculate the CRTC and PLL parameters, and program the
CRTC and PLL parameters.

Created the routine DoWePatchVGAmodes to return if we need to patch the
CRTC parameters for the current VGA mode.

Modified the routine I2CReadByte to preserve DX.

* OEMDATA.ASM *
Renamed the refereces to FLD_CRT to FLD_CRT_ACTIVE.

* OEM.INC *
Renamed the equate FLD_CRT to FLD_CRT_ACTIVE.

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8/04/99 - Ver. 0.16
Added support for centering modes on non-scalable DFP.

Renamed the "Panel" routine to "FixupPanel"

* OEM.ASM *
In FixupPanel, added code to handle progamming the VGA registers for
non-scalable panels.

* OEM.INC *
Modified the EXTREGS structure to handle CRTC settings for CR02, CR03,
CR15, and CR16 for 1024x768 and 1280x1024 panels.

* OEMDATA.ASM *
Expanded the tblExtRegisters table for CR02, CR03, CR15, and CR16
settings for 1024x768 and 1280x1024 panels.

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7/28/99 - Ver. 0.15
Redefined the usage of the scratch registers. Made CR1E for TV data and CR1F for DFP data only. Defination of the scratch register usage is documented in "Scratch Register Usage.XLS".

Created the routine GetPanelSize to read the DFP EDID data to determine the size of the attached panel. The size of the panel is stored in scratch register 2, CR1F.

Created the routine CalcNVRAMchecksum to recalculate the NVRAM checksum after writing data to the NVRAM.

* OEM.ASM *
Moved the CheckForPanel and CheckFPSideScaling routines to OEMPOST.ASM since this is actually once during POST.

Created the routine IsPanelSideScaling to return if the attached panel support panel side scaling.

Modified the GetPanelSize routine to read the panel size from SCRATCH_REG3.

Modified the routine I2CReadByte to PUSH ans POP AX. AX needs to be preserved for the Panel sizing routine.

Modified IsPanelAttached routine to read Scratch Register 2, CR1F, bit 1.

* OEM.INC *
Removed the equates FL_PANEL1280 and FL_PANELSCALING.

Created the following equates for panel size and panel side scaling:
SCRATCH_REG3
CFG_DFP_SIZE_MASK, CFG_DFP_SIZE_1024, CFG_DFP_SIZE_1280, CFG_DFP_SIZE_1600
FLD_EDID_1280, FLD_EDID_1024, FLD_EDID_800
FLD_PANELSCALING

* OEMPOST.ASM *
Created the following routines for reading the panel size:
DeterminePanelSize and CheckIfSupportedPanelSize.

Moved the following routines from OEM.ASM into OEMPOST.ASM:
CheckFPSideScaling and CheckForPanel.

Created the routine CalcNVRAMchecksum which calcaultes and writes the Checksum of the NVRAM to byte offset 127. This routine is called after writing the NVRAM.

In OemNoMonitor, changed thecode to set TV active to use the FLD_TV_ACTIVE equate instead of the 020h value.

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7/23/99 - Ver. 0.14
* OEM.INC *
Updated the Napalm CHIP ID to 07h

* OEMPOST.ASM *
Removed the PUSH and POP BX call from the TV code in InitRegisters.
This fixes the system hang bug when not doing TV autodetection.

* OEMDATA.ASM *
Renamed all the 18Xh mode numbers to 12Xh.
Refer to the document MODELIST.DOC for mode numbers.

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7/22/99 - Ver. 0.13
Fixed bug with 350 scanline modes not being displayed on the TV.

* OEM.ASM *
In FixupTVOut, made sure Misc. Output[7:6] are 11b to force Hsync
and Vsync to positive.

* OEMPOST.ASM *
In InitRegisters, changed the default for no CRT, TV, nor LCD attached
to CRT only.

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7/19/99 - Ver. 0.12
Fixed bug with not being able to compile a TV BIOS.
Modified the routines which read the TV type to read it from the EEPROM
      instead of Scratch Register 2.
During POST, EEPROM byte 0 is read to verify valid TV data is present.
  If TV data isn't valid, EEPROM byte 0 is written with valid TV data.

* OEM.ASM *
Modified IsNTSCMode, IsPALMode, and GetPALMode to read the TV
configuration from the EEPROM byte 0.

Modified routines which checked if composite TV is active to use
the equate FLD_COMPOSITE instead of a hard coded value.

* OEM.INC *
Created the equate FLD_COMPOSITE and CFG_TV_MASK.

* OEMPOST.ASM *
Extern defined the I2C routines to fix problem with not being able to
compile a Napalm TV BIOS.

In InitRegisters, removed the code which set Scratch Register 2 to the
TV mode.

In InitRegisters, added code to verify that EEPROM byte 0 has valid
TV data. If not valid, EEPROM byte 0 is written with valid TV data.

Created the routine I2CWriteAuxEEPROM, for writing data to the EEPROM.

Modified routines which checked if composite TV is active to use
the equate FLD_COMPOSITE instead of a hard coded value.

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7/2/99 - Ver. 0.11
Fixed bug with TV subcarrier signal not properly being generated.

* OEMDATA.ASM *
Modified TVData Tables to add BT869 register corrections for Sub-carrier frequency adjustment of NTSC and PAL outputs.
Voodoo3 PRS#6772

* OEM.ASM *
Added BT869 register writes neccessary to adjust the Sub-carrier frequency so that we will be within 50ppm in NTSC and 25ppm in PAL output.
Voodoo3 PRS#6772

* OEM.INC *
Updated the TVData structure to handle programming the additional Brooktree registers.

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6/23/99 - Ver. 0.10
Fixed bug with some VGA modes not coming up on the TV.

* OEMDATA.ASM *
Modifed all the VGA 320x200 TV modes to use the 320x200 TV parameters.
Fixes bug with 320x200 VGA modes not being displayed on the TV.

* OEM.ASM *
In FixUpTV, Fixed bug in MISC register programming which caused Mode 7 not to display on the TV.

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6/16/99 - Ver. 0.09
Fixed bug with the size 32K BIOS wasn't being patched during POST.
Bug caused by fix for 32K TSR BIOS hang.

* INIT.ASM *
Moved the patch for the 32K ROM BIOS size into the routine Patch32KROM in OEMPOST.ASM.

* MAIN.ASM *
In init_code, made a call to Patch32KROM when compiling a 32K ROM BIOS only.

* OEMPOST.ASM *
Created the routine Patch32KROM to patch the ROM size when compiling a 32K ROM BIOS.

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6/9/99 - Ver. 0.08
Fixed bug with 32K version of the TSR BIOS hanging when loading.

Updated all the bank switching routines to reflect new defination
of Read/Write Appeture in VgaInit0 and VgaInit1

* INIT.ASM *
In the InitBIOS routine, add a conditional compile option around the
32K ROM size patch to compile it into a ROM binary and not a RAM binary.
Fixes bug with 32K TSR hanging while loading.

* OEM.ASM *
Modfied the following bank switch routines to reflect the new Read/Write
Appeture bit definations in VgaInit0 and VgaInit1.
OEMSetBank, OEMSetWBank, OEMGetWBank, OEMSetRBank, OEMGetRBank,
OEMIncBank, OEMIncWBank, OEMDecWBank, OEMIncRBank, and OEMDecRBank.

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5/28/99 - Ver. 0.07
Modified the VESA DDC EDID read routine to read DDC from the panel
when active.

Added code to check if a panel is detected during POST.

Added code to check if we want to force a SVideo/Composite or autodetect
the type of TV attached.

Added to check for if the panel supported Panel side scaling.

* VESA.ASM *
Modified the DDCReadEDID routine to read EDID from the panel when
panel is active.

Created the routine ReadFP_EDID to read EDID data from the panel.

* OEMPOST.ASM *
In OEMNoMonitor, added code to check if a panel is connected.

In OEMInitRegisters, added code to read the NVRAM to determine if we
want to autodetect the TV or force the TV setting.

* OEM.ASM *
Added the routines CheckForPanel and I2CWriteRegister for checking if a
panel is attached.

Added the routines I2CReadBusXBytes and I2CReadByte to read DDC
information from the panel.

Added the routine ChecKFPSideScaling to read the DDC information from
the panel and determine if scaling is supported in the panel.

* OEM.INC *
Created the flag FL_PANELSCALING to set CR1D[5] when panel side scaling
is supported.

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5/21/99 - Ver. 0.06
Updated all the LCD centering parameters so that they are centered on the panel.

Fixed bug in GetExtRegsEntry routine to properly load parameters from the EXTREGS table for 200, 350, and 400 scanline text mode.

* OEM.ASM *
Modified GetExtRegsEntry routine to properly load parameters from the EXTREGS table for 200, 350, and 400 scanline text mode.

* OEMDATA.ASM *
In tblModeDescriptions, changed the internal mode number for modes 00,01,02, 03, to 00, 01, 02, and 03h.

In tblExtRegisters, adjusted all the 1024x768 panel CR04, CR05, CR10, and CR11 settings to center the image on the panel.

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5/17/99 - Ver. 0.05
Fixed bug with Protect mode Set Display Start Address routine, function 07h, not properly detecting the start of Vertical start. This fixes problem with SciTeck Display Doctor not displaying the correct frame rate during the page flipping test.

* OEMDATA.ASM *
Modified the VBE protected mode function, Set Display Start Address, to also look for active display when checking for VSYNC. This will guarantee you will find the start of VSYNC.

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5/11/99 - Ver. 0.04
In the 32K ROM only, moved all the routines that are executed only during POST into the upper 32K of the ROM. These routines will be discarded after VGA POST is executed.

* BIOSEND.ASM *
For the 32K ROM only, added 1500 bytes of padding, db 1500 dup (FFh), to push the BIOS POST past the 32K barrier.

* INIT.ASM *
For the 32K ROM only, added code to patch the ROM size to 32K at C000:0002 and the PCI Info block. This patch isn't executed if the BIOS detects that the ROM size at C000;0002 is set to 64K. This is to work around an issue on the Compaq 5240 machine.

* MAIN.ASM *
Set the 32K ROM size to report a 40K ROM. This is later patched to report 32K by the routine InitBIOS.

* MAKEFILE *
Added the new file OEMPOST.ASM into the build process.
Modified the link process to link INIT.obj and OEMPOST.obj after BIOSEND.obj.

* OEMDATA.ASM *
Modified the compile option for tblExtRegisters table.
Removed the TV parameters for the tblExtRegisters table for a non-TV BIOS.

For the 32K BIOS only, modified the PCI Info block to report a 40K BIOS. This is later patched to report 32K by the routine InitBIOS.

* OEMPOST.ASM *
-= NEW FILE =-
Moved all VGA POST routines into this files. These POST routines are:
OEMInitBIOS
OEMInitWakeUp
OEMNoMonitor
OEMSignOn
InitIOBase
InitRegisters

* OEM.INC *
In the EXTREGS structure, added a LCD and TV compile option for xrTVOutIdx.

* OEM.ASM *
Moved routines which are only needed during POST to OEMPOST.ASM.

Merge the routines GetSubdeviceID and GetSubvendorID into GetSSID.

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5/5/99 - Ver. 0.03
Create one universal ROM for both SDRAM and SGRAM.
Added support for 32Meg and 64Meg of video memory.

* OEM.ASM *
In OEMSignOn, modified the sign on message to also print if SDRAM or SGRAM was detected.

Replaced the SDRAM_BIOS compile option with a call to the routine CheckIfSGRAM in the following routines:
InitRegisters
OEMGetMemSize

Modified OEMSignOn to handle 32Meg and 64Meg sign on message.

Modified OEMGetMemSize to handle return 32Meg and 64Meg of memory installed.

* OEM.INC *
Removed all the conditional compile options for SDRAM.

Removed the "-SD" and "-SG" from the STR_OEMVERSION string.

Created the field FLD_SDRAMBOARD. This is tested against DramInit1 to determine if SDRAM or SGRAM memory.

* OEMDATA.ASM *
Created the strings szSDRAM_Memory and szSGRAM_Memory.

Created the strings sz32768K and sz65536K

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5/4/99 - Ver. 0.02
Added 1280x1024 panel timings.  By default, BIOS assumes a 1024x768 panel
where CR1D[6]=0.  To tell the BIOS a 1280x1024 panel is attached,
CR1D[6]=1.

Fixed bug with some ROM binaries not booting.
Fixes PRS#5619

* OEM.ASM *
Modified the routines GetSubdeviceID and GetSubvendorID to get the offset
to the tblPCIInfo table from read C000:0018 instead of using the
tblPCIInfo label.

Modified the Panel routine to check if a 1280x1024 panel is attached to
determine which set of panel timings to load.

Created the routine GetPanelSize, to return the size of panel currently
attached.

* OEM.INC *
Created the field FL_PANEL1280 for determing when a 1280x1024 panel
is attached.

* OEMDATA.ASM *
Added 1280x1024 panel timings into tblExtRegisters and the XLCD_Patch_Table
table.

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4/30/99 - Ver. 0.01

Initial Version of Napalm BIOS.
Based on the Avenger BIOS version 2.11.

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